UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/598,934	09/15/2006	Seiji Nakahata	039.0075	2278

29453 7590 12/19/2008

Judge Patent Associates
Dojima Building, 5th Floor
6-8 Nishitemma 2-Chome, Kita-ku
Osaka-Shi, 530-0047
JAPAN

EXAMINER	
AHMED, SELIM U	

ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
12/19/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/598,934	NAKAHATA ET AL.	
	Examiner	Art Unit	
	SELIM AHMED	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *11 and 22-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10, 11-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/16/2008 and 09/21/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II, including claims 1-10, and 12-21 in the reply filed on 08/26/2008 is acknowledged.

Priority

2. Acknowledgment is made of applicant's claim priority under PCT/JP2005/08745 filed on 05/13/2005. The certified copy has been filed on 09/15/2006.

Information Disclosure Statement

3. The Information Disclosure Statements filed on 06/16/2008 and 09/21/2006 have been considered.

Oath/Declaration

4. The oath or declaration filed on 09/15/2006 is acceptable.

Drawings

5. The drawings filed on 09/15//2006 are acceptable.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 2, 3, 4, 6, 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Tamura et al (US 2002/0102819; Tamura hereinafter).

With regard to claim 1, Tamura discloses a Group III nitride semiconductor e.g. Figs. 1A-1E crystal manufacturing method, comprising: a step of growing at least one Group III nitride semiconductor crystal 3 (para[0059]) on a starting substrate 1; and a step of separating said Group III nitride semiconductor crystal e.g. Fig. 1D-1E from said starting substrate; characterized in that said Group III nitride semiconductor crystal is 10 um or more but 600 pm or less in thickness, and is 0.2 mm or more but 50 mm or less in width (e.g. para[0059]).

With regard to claim 2, e.g. Figs. 1B-1D of Tamura discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 1, characterized in that the principal face of said Group III nitride semiconductor crystal is smaller in area than the principal face of said starting substrate i.e. 3 is smaller in area than 2.

With regard to claim 3, e.g. Figs. 1B-1D of Tamura discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 1, characterized in that said step of growing at least one said Group III nitride

semiconductor crystal includes: a step of forming on said starting substrate a mask layer 2 having at least one window e.g. Fig. 1B; and a step of growing said Group III nitride semiconductor crystal at least on an open surface of said starting substrate below said window in said mask layer.

With regard to claim 4, e.g. Fig. 5B of Tamura discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 3, characterized in that said window is formed from a group composed of at least two micro-apertures 12.

With regard to claim 6, e.g. Fig. 1D of Tamura discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 1, characterized in that whichever of an etching, lasing, or cleaving method is used in said step of separating from said starting substrate said Group III nitride semiconductor crystal.

With regard to claim 7, e.g. para[0070], Fig. 3 of Tamura discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 1, characterized in that the conformation of said Group III nitride semiconductor crystal is hexagonal-platelike, rectangular-platelike, or triangular-platelike.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 5, 8, 9, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura in view of Usui et al (US 7097920; Usui hereinafter).

With regard to claim 12, Tamura discloses a method of manufacturing a Group III nitride semiconductor device e.g. Figs. 1A-1E, 14A-C comprising: a step of growing at least one Group III nitride semiconductor crystal substrate 3 on a starting substrate 1; a step of growing at least one Group III nitride semiconductor crystal layer on said Group III nitride semiconductor crystal substrate e.g. Fig. 14A, element 21, 22, 23; and a step of separating e.g. Fig. 1D-1E from said starting substrate a Group III nitride semiconductor crystal (e.g. element 3 and element 21,22, 23 of Fig 1 and 14 respectively) that is constituted by said Group III nitride semiconductor crystal substrate and said Group III nitride semiconductor crystal layer; characterized in that said Group III nitride semiconductor crystal is 10 pm or more but 600 pm or less in thickness, and is 0.2 mm or more but 50 mm or less in width (e.g. para[0059]). It would have been obvious to one having ordinary skill in the art at the time of the invention to

include layers 21, 22, 23 of Fig. 14A with layer 3 for predictable result i.e. forming an LED.

With regard to claim 5 or 16, Tamura discloses all of the limitations of claim 1 or 12 respectively with the exception of the Group III nitride semiconductor crystal manufacturing method characterized in that said step of growing at least one said Group III nitride semiconductor crystal includes: a step of disposing at least one seed crystal on said starting substrate; and a step of growing said Group III nitride semiconductor crystal with said seed crystal as its nucleus. However, e.g. in col. 1, lines 36-56 of Usui discloses a step of disposing at least one seed crystal on said starting substrate; and a step of growing said Group III nitride semiconductor crystal with said seed crystal as its nucleus. It would have been obvious to one having ordinary skill in the art at the time of the invention to use such method for higher crystalline quality.

With regard to claim 8 or 19, Tamura discloses all of the limitations of the Group III nitride semiconductor crystal manufacturing method recited in claim 1 or 12 respectively, with the exception of that said Group III nitride semiconductor crystal is grown at a rate of at least 10um/hr but not more than 300 um/hr. However, e.g. in col. 7, line 66 of Usui discloses Group III nitride semiconductor crystal is grown at a rate of at least 10um/hr but not more than 300 um/hr. It would have been obvious to one having ordinary skill in the art at the time of the

invention to grow such a rate to maintain the quality of the crystal at an acceptable level.

With regard to claim 9 or 20, Tamura discloses all of the limitations of claim 1 or 12 respectively with the exception of the Group III nitride semiconductor crystal manufacturing method, characterized in that said Group III nitride semiconductor crystal has an impurity concentration that is not more than 5 x 10^19 cm-3. However, e.g. in col. 7/8, lines 66-3 of Usui disclose doping of the Group III nitride semiconductor crystal but does not mention specific amount of doping concentration. It would have been obvious to one having ordinary skill in the art at the time of the invention to dope the Group III nitride semiconductor crystal with an impurity concentration that is not more than 5 x 10^19 cm-3 for specific conductivity desired for the device.

With regard to claim 13, e.g. Figs. 1B-1D of Tamura discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 12, characterized in that the principal face of said Group III nitride semiconductor crystal is smaller in area than the principal face of said starting substrate i.e. 3 is smaller in area than 2.

With regard to claim 14, e.g. Figs. 1B-1D of Tamura discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 12,

characterized in that said step of growing at least one said Group III nitride semiconductor crystal includes: a step of forming on said starting substrate a mask layer 2 having at least one window e.g. Fig. 1B; and a step of growing said Group III nitride semiconductor crystal at least on an open surface of said starting substrate below said window in said mask layer.

With regard to claim 15, e.g. Fig. 5B of Tamura discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 14, characterized in that said window is formed from a group composed of at least two micro-apertures 12.

With regard to claim 17, e.g. Fig. 1D of Tamura discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 12, characterized in that whichever of an etching, lasing, or cleaving method is used in said step of separating from said starting substrate said Group III nitride semiconductor crystal.

With regard to claim 18, e.g. para[0070], Fig. 3 of Tamura discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 1, characterized in that the conformation of said Group III nitride semiconductor crystal is hexagonal-platelike, rectangular-platelike, or triangular-platelike.

8. Claims 10, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura in view of Usui et al (US 7097920; Usui hereinafter) and further in view of Tsuda et al (US 2003/0136957).

With regard to claim 10 or 21, Tamura in view of Usui discloses all of the limitation of claim 1 or 12 respectively with the exception of the Group III nitride semiconductor crystal manufacturing method, characterized in that an off angle between the principal face of said Group III nitride semiconductor crystal and whichever of its (0001) face, (12OO) face, (1120) face, (1101) face, (1102) face, (1121) face, or (1122) face is 0° or more but not more than 4°. However, e.g. in para[0027] of Tsuda discloses an off angle between the principal face of said Group III nitride semiconductor crystal and whichever of its (0001) face, (12OO) face, (1120) face, (1101) face, (1102) face, (1121) face, or (1122) face is 0° or more but not more than 4°. It would have been obvious to one having ordinary skill in the art at the time of the invention to have such characterization of off-angle in order to achieve good surface morphology.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SELIM AHMED whose telephone number is (571)270-5025. The examiner can normally be reached on 9:00 AM-6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571)272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SA

/Evan Pert/
Primary Examiner, Art Unit 2826